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# Time Table

Tuesday, October 16, 2007

	Room 321A	Room 321B	Room 320A	Room 320B	Room 311	Room 310	Lobby		
08:30-09:30	Registration								
09:30-11:10	Session 9	Session 10	Session 11	Session 12	Tutorial III	Chip Design Contest Session 10:00~16:00	Poster Session B 13:30~15:30		
	Design Methodology II	High Speed Signal Interface and Analog Design	Communication SoC Design II	Processor Architecture and Methodology	Dr. Subhrajit Bhattacharya				
11:10-12:00	Keynote Speech III - Bang-Sup Song, Professor, ECE Department, University of California, San Diego [Room 311]								
12:00-13:30	Lunch								
13:30-15:10	Session 13	Session 14	Session 15	Session 16	Tutorial IV	Chip Design Contest Session 10:00~16:00	Poster Session B 13:30~15:30		
	Design Methodology III	RF IC & MEMs	Design for Multimedia, Display and Image Processing	Low Power Design II	Prof. Hyuk-Jae Lee				
15:10-15:30	Coffee Break								
15:30-17:10	Session 17	Session 18	Session 19	Session 20				Chip Design Contest Session 10:00~16:00	Poster Session B 13:30~15:30
	Testing & Verification II	Sensors & MEMs	Special Topics in Next-Generation Growth Engine Project	Embedded Memories, Methodologies, and MEMs					
17:10-17:30	Closing Ceremony & Award Presentation				[Room 311]				

(Seoul National University, Microinfinity)

10:00~17:30

Chip Design contest Session

Room 310

**CDC-1** Security Camera Processor using One-bit Motion Detection

Jeonghun Kim, Jungwoo Park, Kwangjae Lee, Bongchoon Lee, Konwoo Kwon, Suki Kim (Korea University)

**CDC-2** A new Filter-based Face Detection Algorithm and its Hardware Implementation

Yoon gu Kim, Yong Jin Jeong (Kwangwoon University)

**CDC-3** 32bit RISC Processor with Debug Circuit and Peripherals

Hyun Woo Cho, Kyung Chol Huh, Seung Won Song, Tae Hoon Kim, Koon Shik Cho, Heon Chul Park, Ju Sung Park (Pusan National University, Samsung Electro-Mechanics, Pusan National University)

**CDC-4** Design and verification of 24bit DSP

Chang Won Ryu, Dong Hun Lee, Tae Hoon Kim, Koon Shik Cho, Heon Chul Park, Ju Sung Park (Pusan National University, Samsung Electro-Mechanics, Pusan National University)

**CDC-5** Mixed-mode BPSK Demodulator

Duho Kim, Kwang-chun Choi, Woo-young Choi, Young-kwang Seo, Hyunchin Kim (Yonsei University, Samsung Electronics)

**CDC-6** Efficient Design Method of ROM

Yong-Eun Kim, Ki-Sang Jung, Sun-Ah Hong, Seong-Ik Cho, Jin-Gyun Chung (Chonbuk University)

**CDC-7** A CMOS Hybrid Switching Amplitude

**Modulator for Class-E2 EDGE Polar Transmitters**

Tae-Woo Kwak, Min-Chul Lee, Young-Sub Yuk, Kang-Ho Lee, Hyun-Hee Park, Gyu-Hyeong Cho (KAIST)

**CDC-8** An Ultra Wide Band pHEMT Low Noise Amplifier With Darlington Stage

Jinse Jung, Choon Sik Cho, Jae W. Lee, Jaeheung Kim (Korea Aerospace University, Information and Communications University)

**CDC-9** Image Coprocessor on Mobile Display Panel Integration

Sanghyun Lim, Jaehee You (Hongik University)

**CDC-10** Implementation of Turbo Decoder using SOVA Algorithm

Seok Min Yoon, Hyun Suk Choi, Ki Bo Kim, Jong Tae Kim (Sungkyunkwan University)

**CDC-11** 2.4GHz ZigBee MAC/PHY SoC Implementation

Sinae Ji, Woon Hong Kim, Chulho Chung, Jaeseok Kim (Yonsei University)

**CDC-12** Low-Power High-Performance H.264 Decoder

Sangkwon Na, Woong Hwangbo, Jaemoon Kim, Seunghan Lee, Chong-Min Kyung (KAIST)

**CDC-13** High Speed LVDS Receiver Using Telescopic Amplifier

Kwan Woo Yoo, Jeong Beom Kim (Kangwon National University)

**CDC-14** Implementation of an 11 Gb/s CMOS Demultiplexer Using Redundant Multi-Valued Logic  
Sun Hong Ahn, Jeong Beom Kim (Kangwon National University)

# Mixed-mode BPSK Demodulator

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**Abstract** - A new mixed-mode binary phase shift keying (BPSK) demodulator is demonstrated using a half-rate bang-bang phase detector commonly used in clock and data recovery (CDR) applications. A proto-type chip is realized that can demodulate up to 622Mb/s data at 1.4GHz carrier frequency

**Keywords:** BPSK, tracking, Costas-loop, half-rate bang-bang PD

## 1 Introduction

There are several types of BPSK demodulators. In the analog approach, the carrier signal can be recovered by using a phase-locked loop (PLL) after the received signal is squared [1]. With this scheme, the phase error between the received signal and the recovered carrier signal remains. Costas-loop [2] is another classical analog approach, but it needs analog design costs for filter design and device matching. In the digital approach, several different architectures are possible depending on ADC configuration, but the maximum data rate is limited by the speed of ADC. Digital interpolation schemes [3], which are the most popular digital approach, need GSamples/s ADC to oversample hundreds of Mb/s data, and its realization with CMOS is difficult.

In this paper, we report a new mixed-mode BPSK demodulator with a 1.4GHz carrier frequency that can be used for above-mentioned applications. Our demodulator is based on CMOS so that one-chip solution including all the digital functions is possible.

## 2 Mixed-mode approach

Then the phase detecting characteristics of Costas-loop can be represented as shown in Fig. 1(a). Because BPSK signal changes its phase by  $180^\circ$ , this curve has two lock points separated by  $180^\circ$ . Similar PD characteristics can be realized with a half-rate bang-bang PD, commonly used for CDR applications, as shown in Fig. 1(b).

After synchronization, edges of the sampling clock are aligned to centers of input signal as shown in Fig. 2. In the figure, arrows indicate sampling points of PD. Black arrows are rising edges and white arrows are falling

edges of the sampling clock. Then the bang-bang PD produces output sequence which consists of 10 and 01. BPSK demodulation is done by making decision for high when the sequence is 10, and low when the sequence is 01. This can be easily realized by inverting samples at falling edges of the sampling clock, so that the 10 sequence becomes 11, and the 01 sequence 00. This BPSK demodulation scheme can use any type of CDR architectures using a half-rate PD.

The proposed scheme is mixed-mode demodulator since it uses digital phase detector and analog phase controller. In this scheme, phase synchronizing and symbol detection can be achieved with only 1-bit samplers.

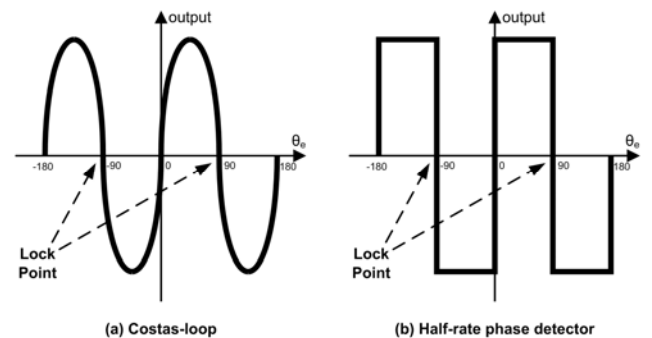


Figure 1. Phase detection characteristic of costas-loop & half-rate bang-bang PD

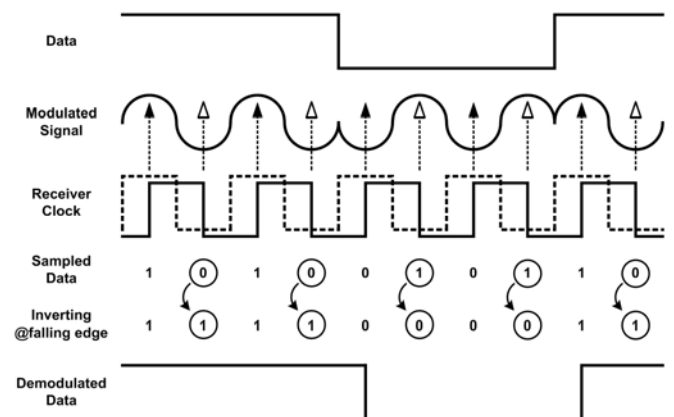


Figure 2. Proposed demodulation scheme

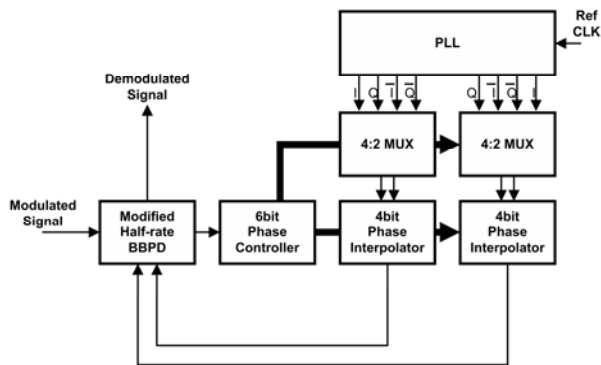


Figure 3. Block diagram of the proto-type chip

Parameter	Value
Process	TSMC 0.18 $\mu\text{m}$
Maximum data rate	622 Mb/s
Carrier frequency	1.4GHz
Demodulator core area	$210 \times 150 \mu\text{m}^2$
Supply Voltage	1.8V
Power Consumption	288mW(including I/O & PLL)

Table 1. Performance of fabricated chip

It means that BPSK signal can be demodulated without ADC. It is easy to extend the proposed scheme to demodulations of higher order PSKs so that they also can be demodulated without ADC. The proposed scheme can also achieve higher data rate because the operating speed of a 1-bit sampler is much faster than ADCs.

### 3 Implementation

The proto-type chip was designed using the phase control algorithm given in [4]. The phase controller has 6bit phase resolution in this design. The control block was implemented by using auto placement and routing with standard CMOS logic cells. Because of low-speed of CMOS logic cells, the clock speed of controller was pulled down to the quarter of the carrier frequency.

The proto-type chip has two analog phase interpolators using the same 6-bit resolution phase controller and different phases from PLL as shown in Fig. 3, because the half-rate bang-bang PD needs multi-phase clocks [5].

### 4 Measurement

The proto-type chip was fabricated using TSMC 0.18  $\mu\text{m}$  CMOS technology. Table 1 shows the performance of the fabricated chip. The maximum error-free data rate achieved in the back-to-back link was 622Mb/s, which is about half of carrier frequency (1.4GHz). Fig. 4 shows 622Mb/s input data (upper) and demodulated data (lower).

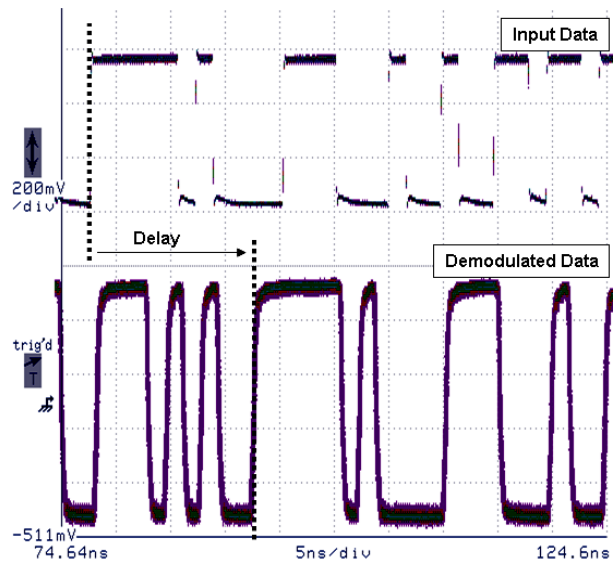


Figure 4. Demodulation for 622Mb/s data

## 5 Conclusion

We demonstrated a new mixed-mode demodulating scheme which can handle a very high data rate compared with the carrier frequency. The demodulator was realized with 0.18  $\mu\text{m}$  CMOS technology. Experimental results show that the proposed scheme can be used for the demodulation of BPSK signals up to 622Mb/s, about half of the carrier frequency.

## References

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